REMARKS

This response responds to the Office Action dated December 15, 2004 in which the Examiner rejected claims 1-7 and 9-31 under 35 U.S.C. §102(b), rejected claim 8 under 35 U.S.C. §103 and rejected claims 1-17 under the judicially created doctrine of obviousness-type double patenting.

Applicants respectfully point out to the Examiner that the copending application Serial No. 10/410,206 is abandoned. Therefore, applicants respectfully request the Examiner withdraws the provisional rejection under the judicially created doctrine of obviousness-type double patenting of claims 1-17.

Claims 1-7 and 9-31 were rejected under 35 U.S.C. §102(b) as being anticipated by *Ooshii* (U.S. Patent No. 5,644,250). In addition, claim 8 was rejected under 35 U.S.C. §103 as being unpatentable over *Ooshii*.

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §102(b) and under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, applicant respectfully requests the Examiner withdraws the rejection to the claim and allows the claim to issue.

Ooshii appears to disclose a semiconductor device, and particularly to a structure capable of easily identifying from an outside of the semiconductor device whether or not an inner circuit is placed under predetermined operating conditions. This invention also relates to a structure for externally identifying whether or not an internal state of a semiconductor device is set so as to satisfy predetermined test conditions. (col. 1, lines 8-15) FIG. 21 is a block diagram showing the structure of an internal voltage down converter shown in FIG. 20. In FIG. 21, an internal voltage

down converter 910 includes a reference voltage generating circuit 922 for generating a reference voltage Vref having a predetermined level, a drive transistor 924 composed of a p channel MOS transistor (insulated gate type field effect transistor) for supplying current to an internal power source line 909 to generate an internal power source voltage VCI from an external power source voltage VCE supplied to a power source line 905, and a comparator 926 for comparing the internal power source voltage VCI on the internal power source line 909 and the reference voltage Vref generated from the reference voltage generating circuit 922 and adjusting the conductance of the drive transistor 924 in accordance with the result of comparison. The comparator 926 receives internal power source voltage VCI at a positive input and reference voltage Vref at a negative input. The internal voltage down converter 910 further includes an n channel MOS transistor 928 which is brought conductive in response to a burn-in mode designation signal BI as an internal state setting signal to electrically connect an output node 929 of the comparator 926 and a ground line 907 to each other. Owing to the provision of the MOS transistor 928, the drive transistor 924 is forcedly brought into a conducting state to equalize the internal power source voltage VCI and the external power source voltage VCE to each other, thereby setting the internal power source voltage VCI to a desired voltage level. An internal power source voltage utilizing circuit 912 includes a load circuit 912a operating with the internal power source voltage VCI on the internal power source line 909 and a ground potential on a ground line 907 as operating power source voltages. The internal power source voltage utilizing circuit 912 includes a plurality of kinds of load circuits 912a for respective functions, to which the internal power source voltage is supplied through different interconnection

lines (for the stabilization of the internal power source voltage due to the dispersion of loads on the power source lines). Therefore, the load circuit 912a included in the internal power source voltage utilizing circuit 912 is representatively shown in FIG. 21. (col. 2, line 44 through col. 3, line 18) In FIG. 2, the semiconductor device includes an internal voltage down converter 910 as an inner circuit, for generating an internal power source voltage VCI, and an internal power source voltage utilizing circuit 912 operating with internal power source voltage VCI as an operating power source voltage which in turn is supplied from internal voltage down converter 910. The internal voltage down converter 910 and the internal power source voltage utilizing circuit 912 are identical in structure to those shown in FIG. 21. The semiconductor device further includes an n channel MOS transistor 20 which is provided between a power pad 10 supplied with an external power source voltage VCE and a ground pad 12 supplied with a ground voltage VSS and which is adapted to form a current path in response to a burn-in mode designation signal BI. In FIG. 2, the n channel MOS transistor 20 is coupled to the power pad 10 through a power source line 905. One conducting terminal (drain) of the MOS transistor 20 may be connected directly to the power pad 10 through an interconnection line different from the power source line 905. The other conducting terminal (source) of the MOS transistor 20 may be connected to the ground pad 12 through an interconnection line different from a ground line 907. Alternatively, the other conducting terminal of the MOS transistor 20 may be connected to the ground pad 12 through the ground line 907. In the normal operation of the semiconductor device, the burn-in mode designation signal BI is at "L" indicative of an inactive state and MOS transistor 928 and MOS transistor 20 are both in an off state. Under this condition, no current

flowing path is formed between the power pad 10 and the ground pad 12. When the internal power source voltage utilizing circuit 912 or a non-illustrated external power source voltage utilizing circuit such as an input/output buffer is activated, a path through which a current IO flows, may be formed between the power pad 10 supplied with the external power source voltage VCE and the ground pad 12 (e.g., a path through which a current consumed in the semiconductor memory device flows upon its standby). When the burn-in mode designation signal BI is at "L" indicative of the inactive state, the internal power source voltage VCI outputted from the internal voltage down converter 910 is maintained at a level of a reference voltage Vref generated from a reference voltage generator 922 by a comparator 926 and a drive transistor 924. When the burn-in test is to be performed, the burn-in mode designation signal BI is set to an "H" indicative of an active state. (col. 8, line 32 through col. 9, line 15) When the burn-in mode designation signal BI is brought to the "H" indicative of the active state, the MOS transistor 928 is turned on so that a node 929 of the internal voltage down converter 910 is set to a ground voltage VSS level. Thus, the drive transistor 924 is completely turned on so that the internal power source voltage VCI on an inner power source line 909 becomes equal to the external power source voltage VCE supplied to the power pad 10, thereby making it possible to vary the internal power source voltage VCI in accordance with the external power source voltage VCE. At this time, the MOS transistor 20 serving as a current path forming means is turned on in response to the burn-in mode designation signal BI that is "H" in level, so that a current path is formed between the power pad 10 and the ground pad 12. Since the MOS transistor 20 has its own inherent on resistance, an additive current Ia is generated in addition to the consumption current

IO generated by the internal power source voltage utilizing circuit 912 and non-illustrated other external power source voltage utilizing circuit or the like included in the semiconductor memory device. When the additive current Ia is externally detected, it is externally identified that the MOS transistor 20 is turned on and the current path has been formed between the power pad 10 and the ground pad 12. When the MOS transistor 20 is brought into an on state, the MOS transistor 928 included in the internal voltage down converter 910 is turned on. It is thus possible to externally identify that the internal power source voltage VCI outputted from the internal voltage down converter 910 has been set to a state in which it can be varied according to the external power source voltage VCE. (col. 9, lines 26-57)

Thus, *Ooishii* merely discloses an internal voltage down converter 910. Nothing in *Ooishii* shows, teaches or suggests a leakage detecting circuit as claimed in claim 1. Rather, *Ooishii* merely discloses a voltage down converter 910. (col. 8, lines 32-41)

Additionally, *Ooishii* merely discloses a reference voltage generating circuit 922 generating a reference voltage Vref. (col. 2, lines 46-48) Nothing in *Ooishii* shows, teaches or suggests a voltage adjust portion for changing an object voltage in response to an adjustment input as claimed in claim 9. Rather, *Ooishii* merely discloses a reference voltage generating circuit 922.

Finally, *Ooishii* merely discloses the operation of the voltage down converter 910 during a normal mode and during a burn-in mode. (col. 8, line 62 through col. 9, line 15, col. 9, lines 26-57) Nothing in *Ooishii* shows, teaches or suggests a) a first write current line having a data write current flow in one of first and second directions, b) a first driver transistor driving the current in a first direction, c) a second

driver transistor driving current in the second direction and d) a first current adjust portion capable of adjusting current amounts independently from each other as claimed in claim 18. Rather, *Ooishii* merely discloses a normal mode and a burn-in mode of a voltage down converter.

Since nothing in *Ooishii* shows, teaches or suggests the invention as claimed in claims 1, 9 and 18, applicant respectfully requests the Examiner withdraws the rejection to claims 1, 9 and 18 under 35 U.S.C. §102(b).

Claims 2-8, 10-17 and 19-31 depend from claims 1, 9 and 18 and recite additional features. Applicant respectfully submits that claims 2-7, 10-17 and 19-31 would not have been anticipated by *Ooishii* within the meaning of 35 U.S.C. §102(b) and claim 8 would not have been obvious over *Ooishii* within the meaning of 35 U.S.C. §103 at least for the reasons as set forth above. Therefore, applicant respectfully requests the Examiner withdraws the rejection to claims 2-7, 10-17 and 19-31 under 35 U.S.C. §102(b) and withdraws the rejection to claim 8 under 35 U.S.C. §103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the

applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

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By: _____
Ellen Marcie Emas
Registration No. 32,131

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620